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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/608,528	06/30/2000	Peter Liao	4103-67101	1133

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EXAMINER	
ALCALA, JOSE H	
ART UNIT	PAPER NUMBER
2841	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/608,528	LIAO ET AL.	
	Examiner	Art Unit	
	Jose H Alcala	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *14-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. This application has been filed with informal drawings, which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

2. The drawings are objected to because: In Figure 6, if reference number 618 is labeling the "Main Printed Circuit Board", there is no need to write that phrase on the figure. In addition if reference number 624 is labeling the "ASIC", there is no need to write that acronym on the figure. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Reference number 666. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Reference number 128 of Figure 1, reference numbers 612 and 616 of Figure 6. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to

avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

5. The Specification is objected to because reference character "124" has been used to designate both "a printed wire or lead" in page 5,line 29 of Specification and "a stub" in page 6,line 1 of Specification. Appropriate correction is required.

6. The Specification is objected to because reference character "126" has been used to designate both "a termination resistor" in page 5,line 30 of Specification and "a length" in page 6,line 1 of Specification. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 1, in line 3, the limitation: "configured for mounting on" is unclear, it should read: "mounted on". In line 4, the limitation: "configured for providing at least a first resistance" is unclear, because it is not including a structural limitation having the desired property, but is just claiming the property by itself. It is further unclear if it is referring to the resistance of the whole circuit board or if there is a resistor or other element having that resistance. In lines 5 and 6, it is not clear where the "at least a first

conductive pathway" begins, is it from the bottom surface of the multi-pin component, from the top surface of the first circuit board, or from the end of a first pin. In addition it is not clear if the "at least a first conductive pathway" goes all the way through the first circuit board, and ends inside the second circuit board or ends on either a top or bottom surface of the second circuit board.

Line 7 is unclear regarding if the phrase "a conductive pathway" is referring to the same "at least a first conductive pathway" of line 5, or is it a second conductive pathway, in which case the limitation of line 5 should be changed to "at least a first and a second conductive pathway". It is not clear if line 7 is referring to a second portion of the "at least a first conductive pathway", in which case the limitation of line 5 should be changed to read "**a portion of** at least a first conductive pathway". In addition, in line 7 the limitation "formed at least partially using said second circuit board" is unclear and is suggesting a process limitation on a product claim, it should be changed to read something like: "located at least partially inside said second circuit board" or "located at least partially on a surface of said second circuit board", or any other way to make it clear.

Additionally in line 8, the phrase: "said first resistance" should be changed to read: "said at least a first resistance".

Regarding Claim 4, it is unclear regarding which of the circuit boards is the claim referring to, when it reads: "said circuit board".

Regarding Claim 6, it is unclear which part of the conductive pathway (or which conductive pathway if there are more than one) is has a second (or third) pathway. In

addition the phrase: "using a via formed in said circuit board" is unclear if the via is the pathway itself, or if there are different elements being claimed.

Regarding Claim 7, the limitation: "said second board is aligned within at least a portion of the region defined by said footprint" is unclear. It is not clear if the limitation means that the second circuit board has at least a portion located under the footprint area of a first surface of a first circuit board, or simply that one is on top of the other.

Regarding Claim 9, line 2 is not clear on which conductive pathway it is referring to (or to what section of the conductive pathway).

Regarding Claim 11, the limitation: "said conductive pathway is less than the sum of the thickness of said first and second circuit board has a " is unclear. It is not clear regarding which conductive pathway it is referring to (or to what section of the conductive pathway). In addition it is further unclear which of the dimensions of the pathway is the one that is less than the sum of the thicknesses of said first and second circuit boards. Is it the thickness of the pathway, the length, etc.?

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

10. Claims 1-3,6-8,10-11 are rejected under 35 U.S.C. 102(a) as being anticipated by Dranchak et al. (US Patent No. 5,953,214). As best understood by the examiner:

Regarding Claim 1, Dranchak teaches an apparatus for providing termination for at least a first pin (pin of reference number 11) of a multi-pin component (reference number 11) to be mounted in a footprint area (area under the component) of a first surface (reference number 22) of a first circuit board (reference number 20), comprising: a second circuit board (reference number 30), configured for mounting on a second surface (reference number 24) of said first circuit board and configured for providing at least a first resistance; at least a first conductive pathway (reference number 29) from said at least a first pin of said multi-pin component to at least a first location of said second circuit board; and a conductive pathway (reference number 31) formed at least partially using said second circuit board, from said first location of said second circuit board to said first resistance.

Regarding Claim 2, Dranchak teaches that the multi-pin component (reference number 11) can be of different varieties (Column 4,line 15) so it is inherent that it comprises an ASIC.

Regarding Claim 3, Dranchak teaches that said resistance is positioned on a surface of said second circuit board (pad 27, has a resistance and is located on a top surface of said second circuit board).

Regarding Claim 6, Dranchak teaches that at least a portion of said conductive pathway includes a via (reference number 29) formed in said first circuit board.

Regarding Claim 7, Dranchak teaches that said second circuit board is **aligned** within at least a portion of the region defined by said footprint (the word aligned, implies

that there is a sort of alignment such as one element being on top of another, see Figure 1).

Regarding Claim 8, Dranchak teaches that a first portion (the portion of reference number 20 located immediately under reference number 11 in Figure 1) of said second circuit board is positioned within the region defined by said footprint and a second portion (the rest of reference number 20 located outside reference number 11 in Figure 1) of said second circuit board is positioned within a region outside said footprint.

Regarding Claim 10, it is inherent that said first pin carries a signal having a frequency greater than about 1 gigahertz.

Regarding Claim 11, Dranchak teaches that each of said first and second circuit boards has a thickness and wherein said conductive pathway (reference number 29) has a thickness less than the sum of the thicknesses of said first and second circuit boards (See Figure 2).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 4,5,9,12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dranchak et al. (US Patent No. 5,953,214). As best understood by the examiner:

Regarding claim 4, Dranchak teaches all the limitations of the instant claimed invention as stated supra for claim 1, and teaches in column 3, lines 41-53 that the second circuit board can have additional circuit elements, which inherently have a resistance.

Dranchak fails to explicitly teach that the element having the resistance is positioned in an interior region of said circuit board. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Dranchak in order to put the element having a resistance in an interior region of said circuit board. Thus, providing additional wirability and/or functionality to the circuit board, while improving the rigidity of the board. In addition it would have been an obvious matter of design choice to put the element having a resistance in an interior region of said circuit board, since applicant has not disclosed that putting it in a specific section of the board solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with the element having a resistance in any region of the board, and it would have been further obvious, since it has been held that rearranging parts of an invention involves only routine skill in the art. See In re Japikse, 86 USPQ 70.

Regarding Claim 5, Dranchak teaches that the resistance can be in a surface (pad 27, has a resistance and is located on a top surface of said second circuit board), but fails to explicitly teach that said resistance is a surface mount resistor. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use

a resistor, since it was known in the art that a resistor of any kind is the best element to use in order to reliably provide a specific resistance value in a printed circuit board.

The limitations the element having the resistance is printed or buried is a product by process limitation. If the product in the product-by-process claims are the same as or obvious from a product of the prior art, the claims are unpatentable even tough the prior product was made by a different process. See In re Thorpe, 227 USPQ 964,966 (Fed.Cir 1985). A "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding Claim 9, Dranchak teaches all the limitations of the instant claimed invention as stated supra for claim 8, and teaches in column 3, lines 41-53 that the second circuit board can have additional circuit elements. In addition Dranchak teaches for the first circuit board (reference number 20) a conductive pathway (reference number 26) going to a location outside the footprint of the element located at the right of Figure 1. Dranchak fails to explicitly teach that said second portion of said second

board provides at least a portion of a conductive pathway to a location of said first circuit board outside said footprint. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify and combine the teachings of Dranchak in order to have at least a portion of a conductive pathway extending to a location of said first circuit board outside said footprint. Thus, electrically connecting said component to any desired conductive element or other component located outside of the footprint under the first component. In addition it would have been further obvious, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. See St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Regarding Claim 12, Dranchak fails to teach that said second circuit board is coupled to said first circuit board by a ball grid array. It is well known in the art and was well known at the time of the invention to use a ball grid array to couple a circuit board to an element or to another circuit board. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a ball grid array to couple and electrically connect said first circuit board to said second circuit board, thus making a more reliable connection by an inexpensive method.

Regarding Claim 13, the limitation that: "said multi-pin component and said second circuit board are coupled to said main circuit board substantially simultaneously" is a product by process limitation, see explanation for Claim 5.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references show some of the elements of the instant claimed invention: Menzies et al. (US Patent No. 5,982,635), Burdick (US Patent No. 5,255,431), Ehman et al. (US Patent No. 6,021,050), Moriyasu et al. (US Patent No. 6,004,657), Garcia (US Patent No. 6,169,663), and Bedos et al. (US Patent No. 6,031,728).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose H Alcala whose telephone number is (703) 305-9844. The examiner can normally be reached on Monday to Friday.

15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on (703) 308-3301. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

16. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JHA
December 12, 2001

Albert W. Paladini 12-12-01

ALBERT W. PALADINI
PRIMARY EXAMINER